REMARKS

Claims 1-31 are pending in the subject application. Claims 1, 20, 26, and 27 have been amended by the present amendment. The amendments are fully supported by the specification as originally filed.

As recited in claims 1, 20, 26, and 27, the Applicants' claimed invention is directed to a shift register for shifting an input pulse in synchronization with a clock signal, the clock signal being smaller in amplitude than a driving voltage of a control circuit. Claims 1, 20, 26, and 27 have been amended to clearly recite that the level shifters increase the voltage of the clock signal (not the driving signal), and then apply the clock signal to the flip flops.

For example, claim 1 specifically recites that each level shifter increases the voltage of the clock signal, and applies the clock signal to the corresponding block of flip flops, except where the level shifter is suspended.

Independent claims 20, 26, and 27 also recite that each level shifter increases the voltage of the clock signal, and applies the clock signal to the flip flops.

Claims 1-31 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent 6,232,945 to Moriyama et al. (hereinafter "Moriyama") in view of U.S. Patent 6,414,670 to Kim. This rejection is respectfully traversed.

Moriyama fails to teach or suggest a shift register having a plurality of level shifters for level-shifting a clock signal, wherein at least one level shifter is provided for a predetermined number/block of flip flops.

As indicated on page 3 of the Final Office Action of January 2, 2004: "Moriyama does not teach a plurality of level shifters for increasing the voltage of the clock signal..."

However, the Kim reference fails to remedy the deficiencies of Moriyama. Specifically, Kim fails to teach or suggest providing one level shifter corresponding to each flip flop or block of flip flops, where each level shifter increases the voltage of the clock signal and applies the clock signal to the corresponding flip flops or block of flip flops.

In Kim, clock generation controlling units 82-1, 82-2, 82-3 ... 82-n determine whether a clock signal is applied to selective gate line drivers (column 5, lines 4-20; FIG. 8). The gate line drivers 81-1, 81-2, 81-3 ... 81-n incorporate level shifters for level shifting the driving signal. There is no teaching or suggestion that level shifters can be used to level shift a clock signal.

There is simply no support in Kim or any other cited art for the Examiner's conclusion that "the level shifters (LS1...LS154) are (as shown in Fig. 2-3) equally applicable for clock signals" (Final Office Action, page 2). In column 2, lines 12-22, Kim teaches that drive signal STV1 "is provided at a first falling edge of the CPV signal (clock signal)," where the drive signal STV1 is shifted; there is no shifting of the clock signal CPV. Column 1, lines 37-50 and FIG. 2 of Kim clearly indicate that the level shifters (LS1 to LS154) level shift a driving signal; there is no teaching or suggestion that such level shifters can be used to level shift a clock signal.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,

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